IEEE-ED NIT Silchar Student Branch Chapter

IEEE-EDS Mini-Colloquium (MQ) on
"Recent Trends in Microelectronics & VLSI Design"

Date: Nov 03, 2018, 09:30 AM, Venue: Virtual Class Room, CCC

Program Schedule

09:30 - 10:00: Inauguration followed by Photo Session

10:00 - 11:30: Lecture by Prof. Manoj Saxena

Title: **Novel Junction-Less Transistor Designs**

11:30-11:45: Tea Break

11:45 -13:15: Lecture by Prof. G. N. Dash

Title: **SiGe Bandgap Engineering for Bipolar VLSI Design**

13:15 -14:15: **Lunch at Guest House**

14:15 -15:45: Lecture by Prof. C. K. Sarkar

Title: **Electronic and Biochemical applications of Green Synthesized Noble Metal Nano particles**

15:45 – 16:00: Tea Break

16:00 – 17:30: Lecture by Prof. A. K. Panda

Title: **Low Power Low Cost ASIC Chip for River Water Quality Monitoring**

17:30 - 18:00: Valedictory

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Brief Profile and Lecture Abstract

Dr. Ajit Kumar Panda, a senior member of IEEE is working as a Professor in National Institute of Science and Technology (NIST), Berhampur. He is a Distinguished Lecturer of IEEE Electron Device Society. He is the Faculty Advisor of IEEE ED NIST Students Chapter. He works on Semiconductor Devices (Focusing on HEMT/MOS HEMT) and Circuits (Focusing on Sensors Interface Circuit Design for use in IoT and glitch minimization).

Low Power Low Cost ASIC Chip for River Water Quality Monitoring

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***Abstract*:** Availability of information on microbial and organic loads in river water is important for evaluating its portability, chemical treatment and use in agriculture and other industrial activities. However, this type of information for Indian River water is not easily available. Recent years have seen increasing trends in field testing of implementation of sensors; however, they do not seem to aid in measuring pathogens, organic compounds in water and water flow rate and lack energy source which can provide them a continuous supply of energy for obtaining real-time data. Although, energy systems are available for ensuring continuous supply of energy to sensors, challenges exist in keeping supply of energy at remote location, sustained at required low voltage as well as in using sources that are cost-effective. Thu at this juncture a low power low cost water quality monitoring system is needed and the speaker will describe their proposed such systems. It will give the overview of different sensors needed for determining water quality parameters as well as water flow characteristics in river; how to integrate these sensors for obtaining water quality parameters using integrated ASIC chip and integrate real-time data for developing an early warning system for protecting human health using distributed analytics and sense making. After such overview of a water quality monitoring system, the speaker will discuss in detail how to develop ASIC chip to interface sensors on input side and cloud on output side.

Dr. Chandan Kumar Sarkar received the D. Phil. degree from the University of Oxford, Oxford, U.K., in 1983. He was also Postdoctoral Research Fellow of the Royal Commission for the Exhibition of 1851 at the Clarendon Laboratory, University of Oxford, from 1983 to 1985. He was a junior fellow of Wolfson College, Oxford. He also held the graduate award at Wolfson College. He was also a Visiting Fellow at the Linkoping University, Linkoping, Sweden, Max Planck Institute at Stuttgart. Germany. He joined Jadavpur University, Kolkata, in 1987 as a Reader in Electronics and Telecommunication Engineering. Subsequently, he became a Professor and the Head of the Department of Physics, and Dean of Faculty of Science at Bengal Engineering Science University (BESU) during 1996-99, Later he once again joined Jadavpur University ETCE Department as a Professor. He has served as a Visiting Professor in many universities such as Tokyo Institute of Technology, Japan, Hong Kong University, Hong Kong. Since 1999, he has been a Professor with the Department of Electronics and Telecommunication and published more than 300 papers in journals of repute and in well-known International Conferences He has guided more than twenty-five PhD candidates. Prof Sarkar is an Associate at University of La Plata, Argentina supported by third World Academy of Sciences (Trieste). He was INSA –ROYAL SOCIETY (UK) visiting scholar at several UK Universities. Dr. Sarkar is the Chair of the IEEE Electron Devices Society (EDS), Calcutta Chapter and the past Vice Chair of IEEE Section. He is presently serving as a Distinguished Lecturer of the IEEE EDS and invited to several countries. He has been elected as IEEE Chair (Elect) for IEEE Calcutta Section.

Electronic and Biochemical applications of Green Synthesized Noble Metal Nano particles

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***Abstract*:** In this presentation, we demonstrate simple and unexplored procedures for green synthesis of noble metal nanoparticles featuring plant extracts and the study of their diverse electronic and biochemical applications. Characterization techniques like ultraviolet visible spectroscopy (UV-Vis), X-ray diffraction (XRD) and high resolution transmission electron microscopy (HRTEM) were used to analyse the production, crystallinity and morphology of bio-reduced nanoparticles. Analytical study of electronic and biochemical properties were performed by following standard protocols. These green synthesized noble metal nanoparticles were found to have potent biochemical and electronic properties which make them attractive choice for future biomedical and environmental applications.

Manoj Saxena is currently Associate Professor in Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi, New Delhi, India. He received B.Sc. (with honors), M. Sc., and Ph.D. degrees from the University of Delhi in 1998, 2000, and 2006 respectively. He has authored or coauthored 270 technical papers in international journals and various international and national conferences. His current research interests are in the areas of analytical modeling, design, and simulation of non-classical MOSFET architectures like silicon-on-nothing, insulated-shallow-extension, grooved/concave-gate, cylindrical gate and Tunnel FET. He is reviewer to many journals including Solid State Electronics, Journal of Physics: D Applied Physics and IEEE TED and EDL. He is Senior Member of IEEE and also Member of Institute of Physics (UK), Institution of Engineering and Technology (UK), National Academy of Sciences India (NASI), Associate of Indian Academy of Sciences, Bangalore member of International Association of Engineers (Hong Kong) and IEEE Electron Device Society-Region 10 SRC Vice Chair (2016-2017). Currently, he is Regional Editor for South Asia, IEEE EDS Newsletter; Member – EDS Board of Governors; EDS Distinguished Lecturer and Fellow-IETE, India. For his voluntary contribution, he has received the outstanding EDS Volunteer recognition from EDS Chapters in the region in 2012.

Novel Junction-Less Transistor Designs

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***Abstract*:** In recent times, as the device length has substantially decreased, novel doping techniques are required for developing concentration gradient at the junctions. The primary advantage of JunctionLess device is the simplicity in fabrication process. The main difference between a Junction Less (JL) transistor and a classical MOSFET is the absence of junctions i.e. uniform doping for the entire length of the device. The device is heavily doped and the doping is of the order of 10^{18} to 10^{19} cm^{-3}. In JL transistor, bulk conduction takes place in contrast with the surface channel conduction in classical MOSFET. In sub-threshold region, JL transistor is fully depleted. As the gate voltage approaches threshold voltage, it becomes partially depleted and when it reaches flat-band voltage, it is fully on. In sub-threshold region, due to depletion, electric field in JL transistor is very high and above threshold, electric field reduces. This is in contrast to Inversion-Mode (IM) MOSFET where electric field is low in sub-threshold region and high after threshold voltage. As the current flow is mainly concentrated at the centre of film, surface scattering is very less which increases mobility and hence current drive in JL transistor. Single Material Double Gate (SMDG) has several advantages as mentioned above but there are some drawbacks due to high doping concentration. It reduces mobility of the carrier which in turn affects drive current and trans-conductance. The above problems can be avoided by

using Dual Material Double Gate (DMDG) JL transistor. DMDG has two metals in two gates having different work functions. Due to different gate materials, potential step profile is created which screens the effect of drain potential variation. Due to this, several advantages like high on-state current, improved trans-conductance and reduced DIBL are observed. These effects have been investigated by developing efficient drain current model for DMDG JL transistor using conformal mapping technique.

Prof. Gananath Dash is superannuated as Professor and Head of the Electron Devices Group from Sambalpur University (Odisha) India in Nov. 2015. He obtained his Ph.D. in 1992 in the area of microwave and millimetre wave devices. Later he developed interest in such diverse fields as DSP for Bioinformatics, medical data mining and Graphene Based Electron Devices. He has more than 37 years of teaching and research experience. He has authored/co-authored more than 220 research papers in International/National Journals and Conference proceedings. He has supervised 10 Ph. D. and 37 M. Phil. Students with some 6 more on the pipeline for their Ph.D. degree in both science and engineering. Dr. Dash has made significant contributions in the development of a simulation method to assess the effect of tunnelling and diffusion current on IMPATT (IMPact Avalanche Transit Time) diode, new design approach for MITATT (MIxed Tunnelling Avalanche Transit Time) and TUNNETT (Tunnelling Transit Time) mode devices, formulation of a noise theory in MITATT diode using computer simulation method and development of a noise theory analytically applicable to mixed mode operation in IMPATT diode. Dr. Dash is not only a Fellow of the Institution of Engineering and Technology (IET) – UK but also a Fellow Assessor of the same Institution. Besides, he is also a Fellow of the Institution of Electronics and Telecommunication Engineers (IETE), India, a Senior Member of the Institution of Electrical and Electronics Engineers- USA (IEEE), and Members of various IEEE societies. He is recognized as a Distinguished Lecturer of the IEEE Electron Devices Society (EDS). He has reviewed extensively for IEEE Transaction on Electron Devices (USA), International Journal of Electronics (U.K.), Circuits, Systems and Signal Processing (Springer), Journal of Computational Electronics (Springer), Journal of Semiconductors (IOP-UK), and Applied Physics – A (Germany). In addition, he has edited a volume of Indian Journal of Physics (Vol. 77A, No. 2, March 2003) and a volume of International Journal of Material Science (ISSN 0973-4589), (Volume 5, Number 5, 2010) as Guest Editor. Dr. Dash has delivered invited talks on more than 25 occasions at different national and international forums and has chaired sessions at several international conferences in India and abroad. Dr. Dash has published a book titled “Electronic Devices and Circuits” which is published by Universities Press, Hyderabad; the first edition has come out of the press in August 2017.

SiGe Bandgap Engineering for Bipolar VLSI Design

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***Abstract*:** Si is a marvelous gift of nature that fits into the growth of the internet age in an amazing way. In fact it has dominated the arena of microelectronics and VLSI design for several decades now. With the entry of the III-V materials into the field, it has become a tough task for the device designers to maintain the dominance of Si. These materials are not only faster than Si but also they are direct bandgaps giving them an edge over Si in optoelectronic applications. In addition, these materials enjoy the flexibility of bandgap engineering which Si is not capable of. In order to address these issues SiGe emerged as the preferred material in the form of SiGe Heterojunction Bipolar Transistors (HBT). SiGe has the advantage of tailor-made bandgap and more importantly it can be integrated into the Si platform for robust VLSI design. Therefore, it will not be surprising that, one day SiGe HBTs would outperform their III-V counterparts. In this DL talk, to begin with, the marvels of Si for microelectronics and VLSI will be outlined. The suitability of SiGe for integration into the Si platform will then be discussed. The encompassing bottlenecks will be resolved. Some SiGe HBTs will be designed and simulated. The results will be discussed. The emerging new ideas on the design criteria of SiGe HBT will be put forth with a conclusion.