About NIT Silchar:

National Institute of Technology, Silchar is one of the 31 National Institutes of Technology of India and was established in 1967 as a Regional Engineering College in Assam. In 2002 it was upgraded to the status of National Institute of Technology and was declared as Institute of National Importance under the National Institutes of Technology Act, 2007. NIT Silchar is a fully residential institution with nine boy's hostels and two girl's hostels. It has six engineering departments and five non-engineering departments.

About Department of ECE:

Department The of Electronics and Communication Engineering is established in 1983. The department has been striving to provide quality technical education since its inception. It offers B. Tech. in Electronics and Communication Engineering and M. Tech. with specializations in Microelectronics & VLSI Design and Communication & Signal Processing. The department also offers Ph.D. programme in various research areas like Micro/Nanoelectronics. VLSI. MEMS/NEMS, Antenna Design, Microwave Engineering, Signal/Image Processing, Wireless Communication Engineering etc.

Eligibility:

This program is open to industrial personnel, faculty members and students including PhD research scholars, PG and UG students of recognized technical institutions.

Registration Procedure:

Interested candidates are advised to fill up the registration form and email the scanned copy of the followings to course coordinator, at Email: <u>ieee.ednits@gmail.com</u> by <u>15th April 2019</u>. (i) Filled in registration form (ii) Identity Card (iii) Proof of Payment

Participants will receive an acknowledgement on acceptance of their application and confirmation of registration over email. All participants have to pay the registration fees before submitting the application through online transfer to the account of **Director, NIT Silchar**, Account No.: **10521277057**, IFSC: **SBIN0007061**, Branch: State Bank of India, NIT Silchar. Brochure and registration form can also be downloaded from institute website: <u>https://www.nits.ac.in</u>

Registration Fees:

*Internal Students: Rs. 500/-*External Students: Rs. 1000/-*Faculty members: Rs. 3000/-*Industry Persons: Rs. 5000/-

Accommodation, Travel and General Information:

All the out station participants will be provided accommodation on payment basis in the Guest House/Hostels of the Institute. No TA and DA will be paid to the participants. Participants will be provided high tea, lunch during the program. Participants will be provided registration kit & course materials.

How to Reach NIT Silchar?

There are daily direct flights to Silchar from Kolkata, Guwahati and New Delhi. Taxis are available from Silchar Airport to NIT Silchar and Silchar is also well connected by Indian Railway and by Road.

Address for Communication:

Dr. T. R. Lenka, Convener Assistant Professor, Department of ECE Mobile: +91-9435387419 Email: <u>trlenka@ece.nits.ac.in</u>

DST-SERB & TEQIP-III Sponsored National Workshop on Modeling of Novel Nanoelectronic Devices and Circuits for ULSI Technology

26st - 30th April 2019

CONVENER Dr. T. R. Lenka Assistant Professor (Grade-I), Dept. of ECE





In Association with IEEE ED NIT Silchar Student Branch Chapter



Department of Electronics & Communication Engineering, National Institute of Technology Silchar (An Institute of National Importance) Silchar, Cachar, Assam, India, 788010 www.nits.ac.in

Course Coverage:

Semiconductor devices are the basic building blocks of VLSI (Very Large Scale Integration) chips. Due to rapid development of semiconductor technology, the dimensions of the electronic devices are shrinking and the density of transistors have increased in the VLSI chips which enables multiple features and functionalities in the electronic gadgets where power, speed and area are the important design metrics. The proportionate change in the device dimensions in the nanometer regime welcomes the ULSI (Ultra Large Scale Integration) Technology worldwide. The nanoscale devices need quantum mechanics (QM) in order to model its electrical and optical behavior. So QM is one of the most important aspect of device modeling for various applications. Hence, it is highly desired to understand the semiconductor device physics and modeling the novel nanoelectronic devices for ULSI Technology. Now-a-days low power circuit design has become a new era in ULSI technology. So it is required to optimize the power dissipation from system level to circuit/device/process level. This workshop will focus on modeling of novel Nanoelectronic devices such as CMOS, TFET, FDSOI, MOS-HEMT, Nanowires, high-k devices etc. based on Si, SiGe, SiC, III-V, II-VI and other emerging electronic materials followed by low power ULSI design.

Tentative List of Resource Persons:

1. Dr. S. C. Bose, Chief Scientist, CEERI, Pilani 2. Prof. Y. S. Chauhan, IIT Kanpur 3. Prof. N. Mohapatra, IIT Gandhinagar 4. Prof. U. Ganguly, IIT Bombay 5. Prof. Sudeb Dasgupta, IIT Roorkee 6. Prof. S. Jit, IIT-BHU, Varanasi 7. Prof. A. K. Panda, NIST, Berhampur 8. Prof. Jawar Singh, IIT Patna

DST-SERB & TEOIP-III Sponsored

National Workshop on **Modeling of Novel Nanoelectronic Devices and Circuits for ULSI Technology**

26st - 30th April 2019 Last Date of Registration: 15th April 2019 Email: ieee.ednits@gmail.com

Registration Form

Name (Block): _____

Gender: MALE / FEMALE

Designation: _____

Organization: _____

Mailing Address: _____

Telephone:

Email: _____

Educational Qualification: _____

Transaction ID:

Bank:_____

Date:_____

Required Accommodation (Paid): YES / NO

Signature of Applicant:

Date:

CHIEF PATRON Prof. Sivaji Bandyopadhyay, Director, NIT Silchar

PATRON Prof. F. A. Talukdar, HoD, Dept. of ECE, NITS

CHAIRMAN Prof. S. Baishya, Dept. of ECE, NIT Silchar

> CONVENER Dr. T. R. Lenka

ORGANIZING COMMITTEE MEMBERS

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> **COORDINATORS Dr. S. K. Tripathy** (Mob: 9465407913) Dr. M. Kavicharan (Mob: 8919656541) Assistant Professor, Dept. of ECE



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